

Claim Rejections - 35 USC §103

In the Office Action, the Examiner now rejects Claims 1-5 and 7-14 under 35 USC §103(a) as being unpatentable over Shimada (US 6,323,051) in view of Suzawa et al. (US 2002/0171085). This rejection is respectfully traversed.

In the rejection, the Examiner contends that “Shimada teaches a semiconductor device (Figure 1d) comprising ... an electrode or a wiring formed by stacking a second conductive layer (2') on the first conductive layer (2) ... But Shimada fails to teach a semiconductor thin film over the substrate and a first conductive layer in contact with the semiconductor thin film. However, Suzawa et al. teaches an additional semiconductor thin film layer (505/1001) over a substrate and in contact with a first conductive layer... Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have included an additional semiconductor thin film in the arrangement claimed by Applicant for the reasons discussed in Suzawa et al.” Applicants respectfully disagree.

In particular, independent Claims 1-5 specifically recite the feature of “an electrode or a wiring formed by stacking a first conductive layer *in contact with the semiconductor thin film* and a second conductive layer on the first conductive layer” (emphasis added). In contrast, it appears that the second conductive layer (2') and the first conductive layer (2) in Shimada are a gate electrode, and the gate electrode is not in contact with the semiconductor films 4-5 since the thin film transistor cannot work if the gate electrode and the semiconductor films 4-5 are in contact with each other. Hence, there is no reason or motivation for one skilled in the art to modify Shimada to contact the semiconductor films with the first conductive layer nor is it clear how Shimada could be modified to have such a structure.

Further, in the present application, it states that “[i]t is an object of the present invention to

connect a wiring, an electrode, or the like formed with two incompatible films (an ITO film and an aluminum film) without increasing the cross-sectional area of the wiring and to achieve lower power consumption even when the screen size becomes larger.” See e.g. paragraph [0014] in the specification of the present application. There is no such suggestion in Shimada since the first and second conductive layers (2 and 2’) in Shimada do not need to contact the semiconductor films 4-5.

Therefore, it is respectfully submitted that there is no reason or motivation to combine Shimada with Suzawa to arrive at the claimed invention.

As stated in MPEP 2143.01, “[i]f proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.”

In addition, as stated in KSR, “[i]n order to combine or modify references in an obviousness rejection, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. See e.g. KSR Int’l Co. v. Teleflex, Inc., 127 S. Ct. 1727, 1741-1742, 82 USPQ 2d 1385 (2007). This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already know. Id

Therefore, since no such reason or motivation exists here, the combination of references and rejection based thereon are improper, and the claims are patentable over the cited references. Accordingly, it is respectfully requested that this rejection be withdrawn.

Conclusion

It is respectfully submitted that the present application is in a condition for allowance and should be allowed.

If any fee should be due for this response, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

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Respectfully submitted,

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